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THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,091	ARAYA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *October 20, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated November 26, 2004. Claims 1-10 were canceled. Claims 11-19 were added. Claims 11-19 of the application are pending and rejected. This office action is made final.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on October 20, 2004 regarding Japanese Office action dated September 7, 2004. The information has been considered in reviewing the claims.

Specification

3. The disclosure is objected to because of the following informalities:

In the amendments to the specification sent on November 26, 2004, in the paragraph beginning on Page 2, Line 8, "verification is made as to whether the sources operate correct or not... verification is made as to whether the sources operate correct or not" appears to be incorrect and it appears that it should be "verification is made as to whether the sources operate correctly or not... verification is made as to whether the sources operate correctly or not".

In the amendments to the specification sent on November 26, 2004, in the paragraph bridging Page 3 and Page 4, "According to an aspect of the invention, these provide a method as defined in independent claim 1" appears to be incorrect and it appears that it should be "According to an aspect of the invention, these provide a method as defined in independent claim 11".

In the amendments to the specification sent on November 26, 2004, in the paragraph beginning on Page 5, Line 17, "FIG. 4 is a flowchart showing procedures of work that are affected by the first embodiment shown in FIG. 2" appears to be incorrect and it appears that it should be "FIG. 4 is a flowchart showing a procedure of work that is affected by the first embodiment shown in FIG. 2".

Original specification, paragraph starting at Page 6, Line 22 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 7, Line 3 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 7, Line 19 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 9, Line 22 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 10, Line 7 and paragraph starting at Page 10, Line 11 refer to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 11, Line 5 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 16, Line 24 refers to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 17, Line 17 and paragraph starting at Page 17, Line 21 refer to simulation platform which should be corrected to simulation program.

Original specification, paragraph starting at Page 18, Line 1 refers to simulation platform which should be corrected to simulation program.

In the amendments to the specification sent on November 26, 2004, in the paragraph beginning on Page 19, Line 11, "As compared with the HDL and assembly languages, the C and C++ language can be used relative small number of lines of code" appears to be incorrect and it appears that it should be "As compared with the HDL and assembly languages, the C and C++ languages can be used relatively small number of lines of code".

Appropriate corrections are required.

Claim Objections

4. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

5. Claims 12 are objected to because of the following informalities:

In claim 12, Line 2, "restructuring the source code based on o the evaluated data transfer; and" appears to be incorrect and it appears that it should be "restructuring the source code based on the evaluated data transfer; and".

In claim 15, Lines 1-3, "wherein in response to the bus traffic, isolation of the source code in elements representing hardware units and elements representing software units is optimized" appears to be incorrect and it appears that it should be "wherein in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized".

In claim 16, Lines 12-14, "structuring the source code in elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said structured source code elements" appears to be incorrect and it appears that it should be "structuring the source code into elements representing at least one of the hardware units and elements representing at least one of the software units for use in the architecture design by compiling said structured source code elements".

In claim 16, Lines 15-16, "calculating the data transfer rate on the bus by executing the compiled source code elements at a simulation program" appears to be incorrect and it appears that it should be "calculating the data transfer rate on the bus by executing the compiled source code elements in a simulation program".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 11-19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7.1 Claim 11, Lines 5-7 state, "structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units" and Lines 13-14 state, "performing said performance evaluation by simulating said modified source code elements and evaluating said data transfer on the bus".

Specification Page 6, Lines 22-25 state, "a simulation program is structured to perform architecture design by using sources ...in simulation program structuring process, the flow proceeds to step A3 to effect isolation of hardware and software". Therefore it is understood that structuring the simulation program involves isolation of the hardware and software.

Specification page 2, Lines 1-7 state, "Prior to actual manufacturing, simulation programs (or algorithms) are normally structured without consideration of distinctions between hardware and software... Next, isolation of hardware and software is performed on the structured simulation programs, which are divided into hardware elements and software elements respectively. The isolation of hardware and software is made by experiments".

The simulation program is a software tool and it is not hardware. Therefore the structuring of simulation platform involving ***isolation of hardware and software*** mentioned in Specification, Page 6, Lines 22- 25 is not understood. One of ordinary skill in the art will understand that bus operations involve both bus hardware and bus operational software. There is much interaction between hardware and software. Any simulation model of the bus operation will involve both the hardware models and the software models. Therefore it is not understood as to why one will isolate hardware and software in any simulation model of bus operations and how it will affect the simulated bus performance. It is also not understood as to how "The isolation of hardware and software is made by experiments". The specification does not state as to what criteria and process are used to isolate the hardware and software during structuring the simulation program. Therefore the process of structuring the simulation program is not properly described in the specification.

In view of the lack of proper description of the structuring process in the specification, "structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units" is not understood.

In addition, the statement, "isolating elements of said source code representing hardware units and software units" is ***new material*** not found in the original specification and therefore is not given patentable weight.

7.2 Claim 11, Lines 11-12 state, "modifying at least one element of said source code elements based on a result of an implementation of said evaluation function". The specification does not describe the result of implementation of the evaluation function. This is ***new material*** not found in the original specification and therefore is not given patentable weight.

7.3 Claim 12 refers to, "restructuring the source code based on o the evaluated data transfer; and performing said performance evaluation again by simulating said restructured source code again". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above.

7.4 Claim 14 refers to, "feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in said source code new elements representing hardware units and new elements representing software units". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above.

In addition, the statement, "isolating in said source code new elements representing hardware units and new elements representing software units" is ***new material*** not found in the original specification and therefore is not given patentable weight.

7.5 Claim 15 refers to "isolation of the source code in elements representing hardware units and elements representing software units". This is ***new material*** not found in the original specification and therefore is not given patentable weight.

7.6 Claim 16, Lines 12-14 refer to, "structuring the source code in elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said structured source code elements". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above.

In addition, the statement, "in elements representing at least one of the hardware units and the software units" is ***new material*** not found in the original specification and therefore is not given patentable weight.

7.7 Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

8. Claims 15 and 17 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

8.1 Claim 15 states, "in response to the bus traffic, isolation of the source code in elements representing hardware units and elements representing software units is optimized". The specification does not describe anywhere how this isolation of the source code in elements representing hardware units and elements representing software units is optimized. It does not describe the objective function and the process used for optimization of isolation of the source code in elements.

8.2 Claim 17 states, "the variables loaded onto the bus consist of n bits while the bus consists of m bit lines, where n and m are both integers, and n is a multiple of m, and the bus traffic for the processing rate is produced such that the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate". It is not understood as to why "a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate" and how it affects the bus traffic or the processing rate evaluations and the design of the bus architecture. The specification does not state why "a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate" and how it affects the bus traffic or the processing rate evaluations and the design of the bus architecture.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 11-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al.** (U.S. Patent 6,269,467) in view of **Tseng et al.** (U.S. Patent 6,321,366), and further in view of **Swoboda et al.** (U.S. Patent 6,546,505) and **Fujiwara et al.** (U.S. Patent 6,510,541).

11.1 **Chang et al.** teaches block based design methodology. Specifically, as per claim 11, **Chang et al.** teaches a method in a LSI design and development process for evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of the design and development process (CL27, L14-27; CL27, L29-31; CL29, L17-22; CL29, L29-35); the method comprising:

performing the performance evaluation by simulating the modified source code elements and evaluating the data transfer on the bus (CL29, L29-35; CL52, L6-8; CL52, L29-37; CL52, L47-50; CL33, L53-59; CL40, L16-19).

Chang et al. does not expressly teach structuring source code by isolating elements of the source code representing hardware units and software units. **Tseng et al.** teaches structuring source code by isolating elements of the source code representing hardware units and software units (CL36, L11-20; CL39, L39-41), because that allows the system to deliver data between the software model and the hardware model (CL36, L11-13) and selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that included structuring source code by isolating elements of the source code representing hardware units and software units. The artisan would have been motivated because that would allow the system to deliver data between the software model and the hardware model and selective control of data delivery across the software/hardware boundary.

In addition, **Fujiwara et al.** teaches structuring source code by isolating elements of the source code representing hardware units and software units (Fig. 2, Item 302; CL8, L13-14; CL8, L42-44; CL9, L60-61), because each specification is described with a language capable of representing state transfer logic (CL8, L21-23); data stored in hardware section is described with a hardware description language such as Verilog or VHDL and data stored in software section is described in C/C++ source code (CL10, L9-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Fujiwara et al.** that included structuring source code by isolating elements of the source code representing hardware units and software units. The artisan would have been

motivated because each specification would be described with a language capable of representing state transfer logic; data stored in hardware section would be described with a hardware description language such as Verilog or VHDL and data stored in software section would be described in C/C++ source code.

Chang et al. does not expressly teach describing the algorithm design in a general purpose high-level programming language. **Swoboda et al.** teaches describing the algorithm design in a general purpose high-level programming language (CL5, L42-44; CL5, L56-60), because the high level language code is tailored according to the needs of a given application (CL5, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Swoboda et al.** that included describing the algorithm design in a general purpose high-level programming language. The artisan would have been motivated because the high level language code could be tailored according to the needs of a given application.

Chang et al. does not expressly teach creating an evaluation function for evaluating data transfer that occurs on the at least one bus. **Tseng et al.** teaches creating an evaluation function for evaluating data transfer that occurs on the at least one bus (CL14, L63 to CL15, L1; CL61, L18-23; CL101, L67 to CL102, L3), because to evaluate data, data is transferred from main memory in the host processor to the hardware elements via the bus (C61, L18-20). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that included creating an evaluation function for evaluating data transfer that occurs on the at least one bus. The artisan would have

been motivated because to evaluate data, data would be transferred from main memory in the host processor to the hardware elements via the bus.

Chang et al. does not expressly teach the bus being a part of the source code realizing the data transfer between the elements representing hardware units and software units. **Tseng et al.** teaches the bus being a part of the source code realizing the data transfer between the elements representing hardware units and software units (CL36, L11-20; CL39, L39-41), because that allows the system to deliver data between the software model and the hardware model (CL36, L11-13) and selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that included the bus being a part of the source code realizing the data transfer between the elements representing hardware units and software units. The artisan would have been motivated because that would allow the system to deliver data between the software model and the hardware model and selective control of data delivery across the software/hardware boundary.

Chang et al. teaches modifying at least one element of the source code elements based on a result of a simulation (CL52, L6-8; CL52, L20-28). **Chang et al.** does not expressly teach modifying at least one element of the source code elements based on a result of an implementation of the evaluation function. **Tseng et al.** teaches modifying the sources by executing a specific evaluation function (CL14, L63 to CL15, L1; CL4, L28-33; CL61, L16-23), because evaluation data transfer among logic devices occurs across the interconnects and the buses (CL102, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that

included modifying the sources by executing a specific evaluation function. The artisan would have been motivated because evaluation data transfer among logic devices would occur across the interconnects and the buses.

11.2 As per claim 12, **Chang et al., Tseng et al., Swoboda et al.** and **Fujiwara et al.** teach the method of Claim 11. **Chang et al.** teaches performing the performance evaluation again by simulating the restructured source code again (CL29, L29-35; CL52, L6-8; CL52, L29-37; CL52, L47-50; CL33, L53-59; CL40, L16-19).

Chang et al. teaches restructuring the source code based on (CL52, L6-8; CL52, L20-28). **Chang et al.** does not expressly teach restructuring the source code based on the evaluated data transfer. **Tseng et al.** teaches restructuring the source code based on the evaluated data transfer (CL14, L63 to CL15, L1; CL4, L28-33; CL61, L16-23), because evaluation data transfer among logic devices occurs across the interconnects and the buses (CL102, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the of **Chang et al.** with method of **Tseng et al.** that included restructuring the source code based on the evaluated data transfer. The artisan would have been motivated because evaluation data transfer among logic devices would occur across the interconnects and the buses.

11.3 As per claim 13, **Chang et al., Tseng et al., Swoboda et al.** and **Fujiwara et al.** teach the method of Claim 11. **Chang et al.** teaches that a bus traffic is calculated from the evaluated

data transfer with respect to the processing rate of the bus (CL29, L29-35; CL33, L53-59; CL40, L16-19).

11.4 As per claim 14, **Chang et al., Tseng et al., Swoboda et al.** and **Fujiwara et al.** teach the method of Claim 11. **Chang et al.** teaches feeding back a result of the performance evaluation of the bus to the step of structuring the source code (CL52, L6-8; CL52, L20-28; Cl52, L29-37; CL52, L47-50); to improve the architecture design at a high-level design stage (CL27, L14-27; CL27, L29-31; CL29, L17-22; CL29, L29-35).

Chang et al. does not expressly teach improving the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units. **Tseng et al.** teaches improving the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units (CL36, L11-20; CL39, L39-41), because that allows the system to deliver data between the software model and the hardware model (CL36, L11-13) and selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that included improving the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units. The artisan would have been motivated because that would allow the system to deliver data between the

software model and the hardware model and selective control of data delivery across the software/hardware boundary.

11.5 As per claim 15, **Chang et al., Tseng et al., Swoboda et al.** and **Fujiwara et al.** teach the method of Claim 14. **Chang et al.** does not expressly teach that in response to the bus traffic, isolation of the source code in elements representing hardware units and elements representing software units is optimized. **Tseng et al.** teaches that in response to the bus traffic, isolation of the source code in elements representing hardware units and elements representing software units is optimized (CL36, L11-20; CL39, L39-41), because that allows the system to deliver data between the software model and the hardware model (CL36, L11-13) and selective control of data delivery across the software/hardware boundary (CL39, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chang et al.** with the method of **Tseng et al.** that included in response to the bus traffic, isolation of the source code in elements representing hardware units and elements representing software units being optimized. The artisan would have been motivated because that would allow the system to deliver data between the software model and the hardware model and selective control of data delivery across the software/hardware boundary.

11.6 As per claim 18, **Chang et al., Tseng et al., Swoboda et al.** and **Fujiwara et al.** teach the method of Claims 11 to 15. **Chang et al.** does not expressly teach that the general purpose high-level language is one of C language and C++ language. **Swoboda et al.** teaches that the general purpose high-level language is one of C language and C++ language (CL5, L42-44;

CL5, L56-60), because the high level language code is tailored according to the needs of a given application (CL5, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the bus performance evaluation method of **Chang et al.** with the bus performance evaluation method of **Swoboda et al.** that included the general purpose high-level language being is one of C language and C++ 1anguage. The artisan would have been motivated because the high level language code would be tailored according to the needs of a given application.

Conclusion

ACTION IS FINAL

12. Applicant's amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 25, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER